Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:

simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in ~~an~~ the good integrated circuit device design;

simulating ~~a test of~~ said integrated circuit device test to test said simulated flawed integrated circuit device design; and

determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design.

2. (Canceled)

3. (Currently Amended) [[A]] The method ~~in accordance with claim 2~~ of claim 3, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

4. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 1, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed

integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

5. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 1, further comprising the ~~first~~ step of:

~~generating~~ simulating said good integrated circuit device design ~~that meets specifications of said integrated circuit device~~.

6. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 5, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass

~~verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design~~.

7. (Currently Amended) [[A]] The method in accordance with claim 6, wherein ~~further comprising~~:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws ~~modeling said one or more chip defects with said one or more known flaws~~.

8. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 7, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

9. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 1, ~~first~~ comprising the step of:

modifying said good integrated circuit device design to include said one or more known physical flaws to generate said flawed integrated circuit device design.

10. (Canceled)

11. (Canceled)

12. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 9, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

13. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 9, further comprising the first step of:

~~generating~~ simulating said good integrated circuit device design ~~that meets specifications of said integrated circuit device~~.

14. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 13, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass

~~verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design~~.

15. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 14, wherein ~~further comprising~~:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws ~~modeling said one or more chip defects with said one or more known flaws~~.

16. (Currently Amended) [[A]] The method ~~in accordance with~~ of claim 15, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

17. (Currently Amended) A computer readable storage medium tangibly embodying program instructions implementing a method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:

simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in ~~an~~ the good integrated circuit device design;

simulating ~~a test of~~ said integrated circuit device test to test said simulated flawed integrated circuit device design; and

determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design.

18. (Canceled)

19. (Currently Amended) The computer readable storage medium of claim 17 ~~18~~, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

20. (Currently Amended) The computer readable storage medium of claim 17, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

21. (Currently Amended) The computer readable storage medium of claim 17, further comprising the first step of:

~~generating~~ simulating said good integrated circuit device design ~~that meets specifications of said integrated circuit device~~.

22. (Currently Amended) The computer readable storage medium of claim 21, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass

~~verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design~~.

23. (Currently Amended) The computer readable storage medium of claim 22, wherein ~~further comprising~~:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws ~~modeling said one or more chip defects with said one or more known flaws~~.

24. (Currently Amended) The computer readable storage medium of claim 23, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

25. (Currently Amended) The computer readable storage medium of claim 17, ~~first~~ comprising the step of:

modifying said good integrated circuit device design to include said one or more known flaws to generate said flawed integrated circuit device design.

26. (Canceled)

27. (Canceled)

28. (Currently Amended) The computer readable storage medium of claim 25, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

29. (Currently Amended) The computer readable storage medium of claim 25, further comprising the ~~first~~ step of:

~~generating~~ simulating said good integrated circuit device design ~~that meets specifications of said integrated circuit device~~.

30. (Currently Amended) The computer readable storage medium of claim 29, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass

~~verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design~~.

31. (Currently Amended) The computer readable storage medium of claim 30, wherein ~~further comprising~~:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws ~~modeling said one or more chip defects with said one or more known flaws~~.

32. (Currently Amended) The computer readable storage medium of claim 31, further comprising the step of:

indicating that said integrated circuit device test ~~of said simulated flawed integrated circuit device~~ is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more ~~of said~~ known physical flaws in said simulated flawed integrated circuit device design.

33. (Currently Amended) An integrated circuit device test verification apparatus, comprising:

an integrated circuit device simulator which simulates a flawed integrated circuit device design, said flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good ~~of an~~ integrated circuit device design;

a tester simulator which simulates a an integrated circuit device test executing on an integrated circuit device tester that generates test stimuli, applies said generated test stimuli to said simulated flawed integrated circuit device design, and receives test responses from said simulated flawed integrated circuit device design; and

a simulated test results analyzer which determines whether said simulated integrated circuit device test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said flawed integrated circuit device design.

34. (Canceled)

35. (Currently Amended) [[An]] The integrated circuit device test verification apparatus ~~in accordance with~~ of claim [34] 33, wherein:

said simulated test results analyzer determines that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

36. (Currently Amended) [[An]] The integrated circuit device test verification apparatus ~~in accordance with~~ of claim 33, wherein:

said integrated circuit device simulator also simulates ~~a known~~ said good integrated circuit device ~~of an integrated circuit device~~ design;

said tester simulator simulates said integrated circuit device test executing on said integrated circuit device tester, and applies said generated test stimuli to said simulated good integrated circuit device design, and receives test responses from said simulated good integrated circuit device design; and

said simulated test results analyzer determines whether said simulated test of said simulated ~~known~~ good integrated circuit device design passes said simulated ~~known~~ good integrated circuit device design.

37. (Currently Amended) [[An]] The integrated circuit device test verification apparatus ~~in accordance with~~ of claim 36, wherein:

said simulated test results analyzer determines that said integrated circuit device test is flawed if said simulated test of said simulated ~~flawed~~ good

integrated circuit device design does not pass said simulated ~~known~~ good integrated circuit device design.